

The following is a complete listing of all claims in the application, with an indication of the status of each:

Listing of claims:

- 1 1. (currently amended) A multichip circuit module having a main circuit
2 board, at least one carrier substrate mounted on the main circuit board and
3 which is in electrical contact with the main circuit board, and at least one
4 semiconductor chip on the carrier substrate which is in electrical contact with
5 the carrier substrate, wherein
6 the carrier substrate has at least one cavity on a mounting surface to
7 accommodate said at least one semiconductor chip, the carrier substrate
8 having a plurality of layers with conductor tracks extending transversely
9 through said plurality of layers and terminating in conductor contacts on said
10 mounting surface.
11 connecting contacts for associated bumps of said at least one
12 semiconductor chip are provided in said at least one cavity,
13 the at least one semiconductor chip being mounted on the connecting
14 contacts by using the associated bumps in a flip-chip technique, and
15 the mounting surface of the carrier substrate being applied to a contact
16 surface of the main circuit board ~~and the mounting surface of the carrier~~
17 ~~substrate wherein the carrier substrate has many layers with conductor tracks~~
18 ~~extending transversely through a plurality of layers, and via a filling material~~
19 ~~that provides i) a heat dissipation path from makes contact with a rear of said~~
20 at least one semiconductor chip in said at least one cavity to said circuit board
21 and ii) electrical connection between said conductor contacts and

22 corresponding contacts on said circuit board, without enclosing the connecting
23 contacts and bumps.

1 2. (previously presented) The multichip circuit module as claimed in claim 1,
2 wherein the filling material is an anisotropically conductive material.

1 3. (previously presented) The multichip circuit module as claimed in claim 1
2 wherein the filling material does not fill the interspaces of the at least one
3 cavity completely.

1 4. (currently amended) The multichip circuit module as claimed in claim 1
2 wherein the conductor tracks of the carrier substrate are led to the mounting
3 surface and are connected electrically and mechanically to conductor tracks of
4 the main circuit board, and wherein said filling material provides insulation
5 within the filling material between said conductor contacts and encapsulation
6 of said at least one semiconductor chip, thereby providing for the
7 simultaneous carrying of signals, dissipation of heat, encapsulation and
8 shielding.

1 5. (previously presented) The multichip circuit module as claimed in claim 1
2 further comprising a planar antenna arrangement on an underside of the
3 carrier substrate, which is opposite the mounting surface.

1 6. (previously presented) The multichip circuit module as claimed in claim 1
2 wherein the carrier substrate is a multilayer ceramic.

1 7. (currently amended) A method for production of multichip circuit modules
2 having a main circuit board, at least one carrier substrate mounted on the main

3 circuit board and which is in electrical contact with the main circuit board,
4 and at least one semiconductor chip on the carrier substrate which is in
5 electrical contact with the carrier substrate, wherein

6 the carrier substrate has at least one cavity on a mounting surface to
7 accommodate said at least one semiconductor chip, the carrier substrate
8 having a plurality of layers with conductor tracks extending transversely
9 through said plurality of layers and terminating in conductor contacts on said
10 mounting surface.

11 connecting contacts for associated bumps of said at least one
12 semiconductor chip are provided in said at least one cavity,

13 the at least one semiconductor chip being mounted on the connecting
14 contacts by using the associated bumps in a flip-chip technique, and

15 the mounting surface of the carrier substrate being applied to a contact
16 surface of the main circuit board ~~and the mounting surface of the carrier~~
17 ~~substrate wherein the carrier substrate has many layers with conductor tracks~~
18 ~~extending transversely through a plurality of layers, and via a filling material~~
19 ~~that provides i) a heat dissipation path from~~ to said circuit board
20 and ii) electrical connection between said conductor contacts and
21 corresponding contacts on said circuit board. without enclosing the connecting
22 contacts and bumps, having the following steps:

23
24 a) letting the at least one semiconductor chip into cavities provided for
25 semiconductor chips on a mounting surface of the carrier substrate;

26 b) mounting the at least one semiconductor chip by making contact
27 with the bumps of the at least one semiconductor chip to connecting contacts
28 in the cavities using a flip-chip technique;

29 c) applying a layer of filling material to the contact surface of the main
30 circuit board; and

31 d) applying the carrier substrate having the mounting surface to the
32 contact surface of the main circuit board.

1 8. (previously presented) The method as claimed in claim 7 wherein said
2 applying a layer of filling material step is performed by application of an
3 anisotropically conductive filling material to the contact surface.

1 9. (previously presented) The method as claimed in claim 7 wherein said
2 applying a layer of filling material step includes application of the filling
3 material in a layer thickness which is matched in such a way that interspaces
4 of the cavities are not filled completely with the filling material.

1 10. (previously presented) The method as claimed in claim 7 further
2 comprising the step of electrically connecting the conductor tracks, which
3 extend transversely through a plurality of layers of the carrier substrate and
4 are led to the mounting surface to conductor tracks of the main circuit board.

1 11. (previously presented) The method as claimed in claim 7 wherein the
2 steps are performed in a gas atmosphere in order to enclose gas in the cavities.

1 12. (previously presented) The multichip circuit module of claim 2 wherein
2 said anisotropically conductive material is selected from the group consisting
3 of an anisotropically conductive paste and an anisotropically conductive film.

1 13. (previously presented) The multichip circuit module as claimed in claim
2 2 wherein the filling material does not fill the interspaces of the at least one
3 cavity completely.

- 1 14. (previously presented) The multichip circuit module as claimed in claim
2 6 wherein said multilayer ceramic is a low-temperature co-fired ceramic
3 (LTCC).
- 1 15. (previously presented) The method as claimed in claim 7 wherein said
2 anisotropically conductive filling material is a paste or a film.
- 1 16. (previously presented) The method as claimed in claim 8 wherein said
2 applying a layer of filling material step includes application of the filling
3 material in a layer thickness which is matched in such a way that interspaces
4 of the cavities are not filled completely with the filling material.
- 1 17. (previously presented) The method as claimed in claim 8 wherein the
2 steps are performed in a gas atmosphere in order to enclose gas in the cavities.
- 1 18. (previously presented) The method as claimed in claim 9 wherein the
2 steps are performed in a gas atmosphere in order to enclose gas in the cavities.
- 1 19. (previously presented) The method as claimed in claim 10 wherein the
2 steps are performed in a gas atmosphere in order to enclose gas in the cavities.